

*Fig. 1*

FIG. 2A is a schematic diagram of a first embodiment of a device. The device includes a first input terminal (B1) and a second input terminal (B2). The first input terminal (B1) is connected to a first input of a first logic element (LS). The second input terminal (B2) is connected to a second input of the first logic element (LS). The output of the first logic element (LS) is connected to a first input of a second logic element (LS). The second input of the second logic element (LS) is connected to a second input terminal (B2). The output of the second logic element (LS) is connected to a first input terminal (B1). The first input terminal (B1) and the second input terminal (B2) are connected to a common ground terminal (GND).

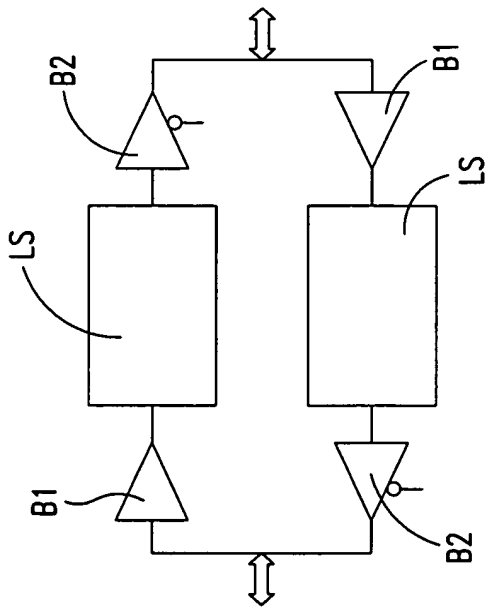


Fig. 2A

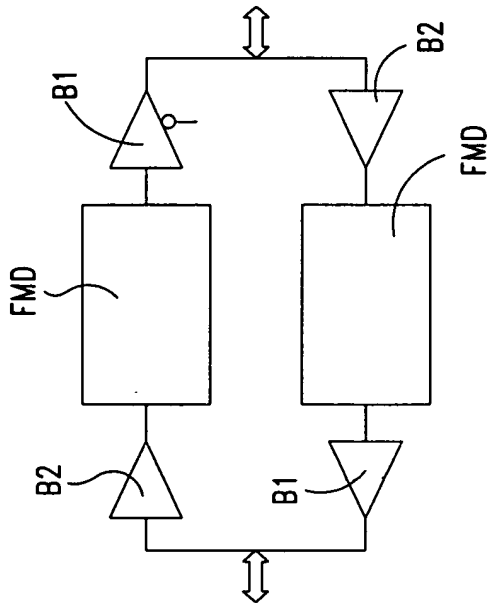


Fig. 2B

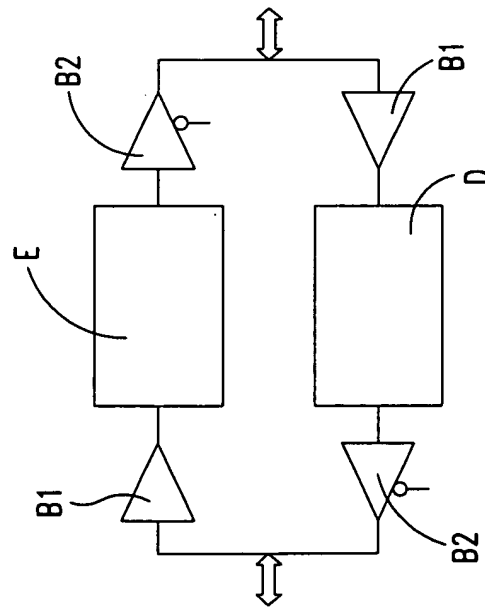


Fig. 2C

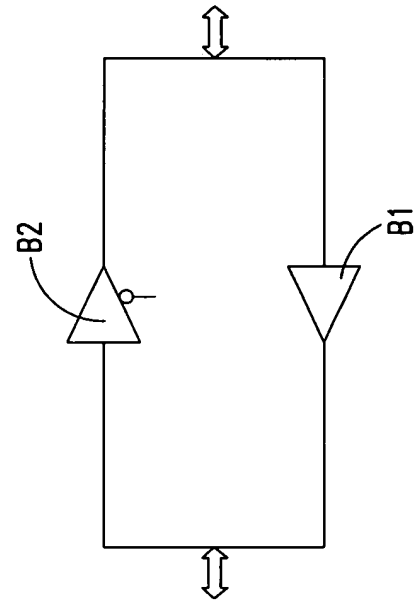
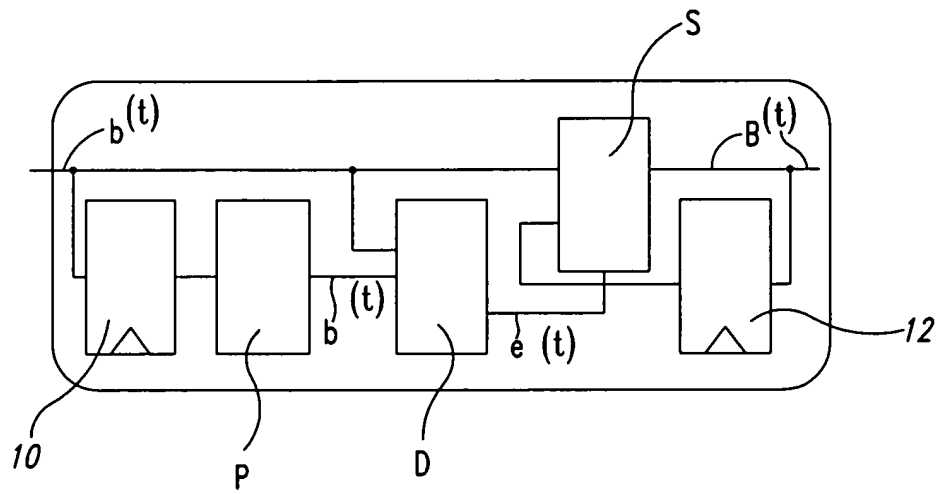
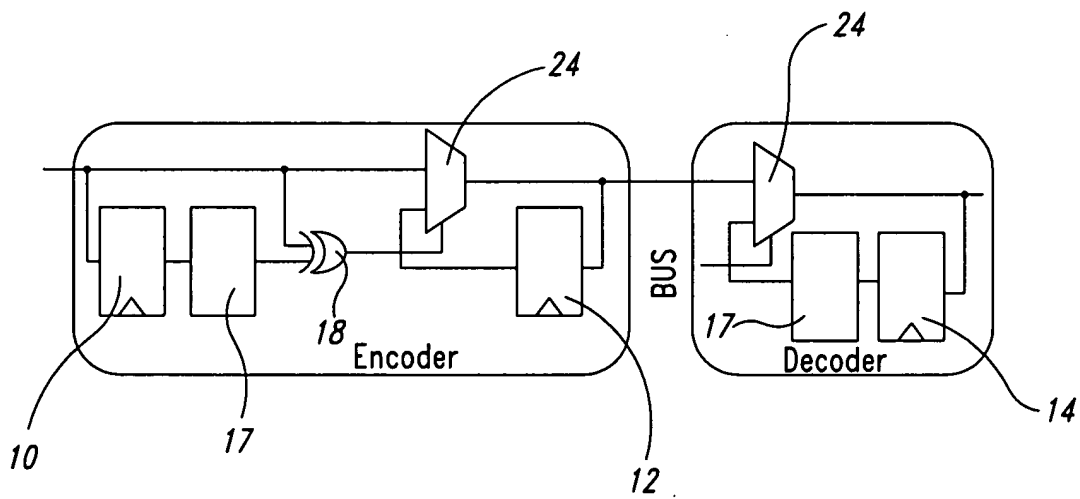


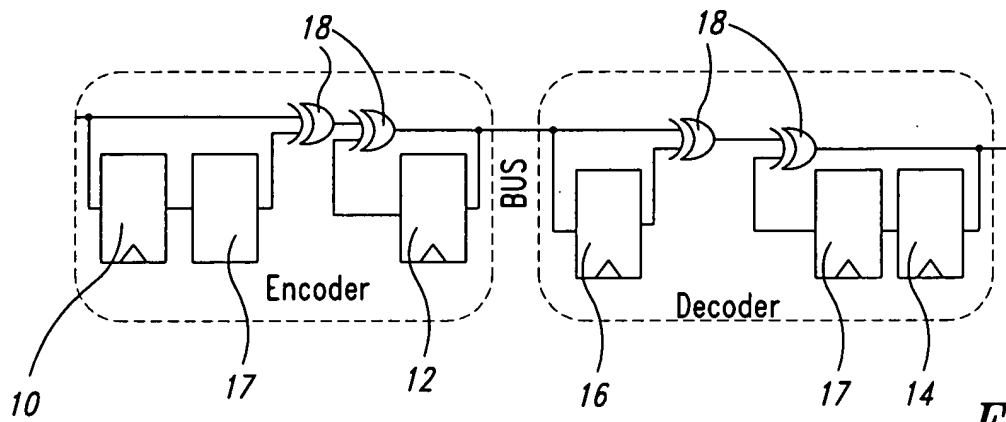
Fig. 2D



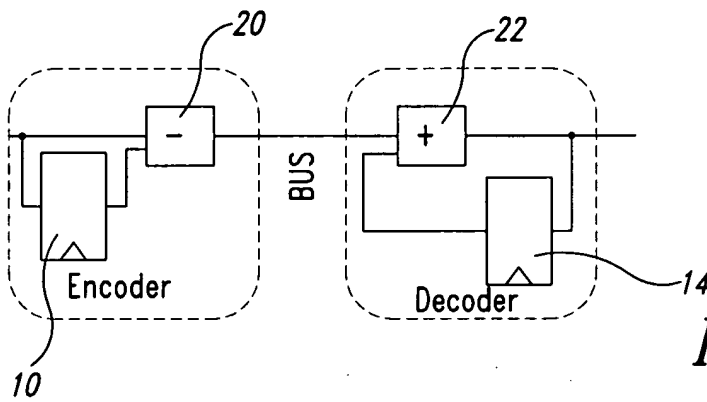
*Fig. 3*



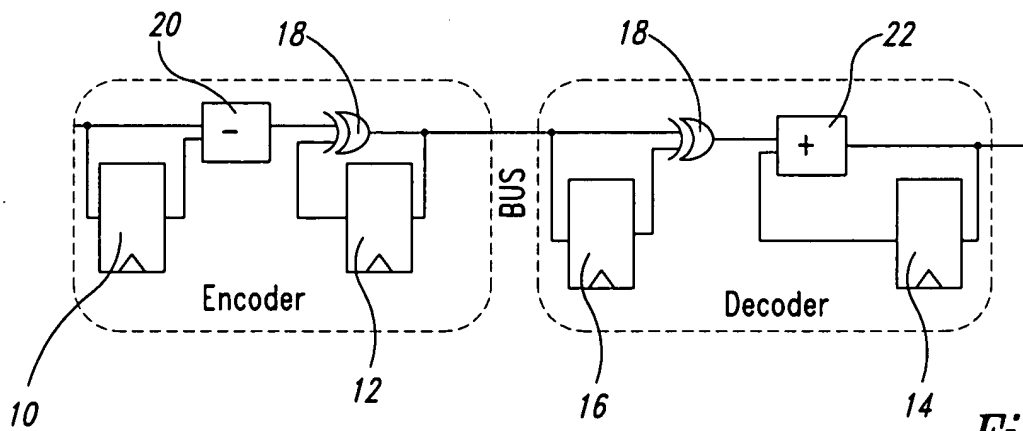
*Fig. 4*



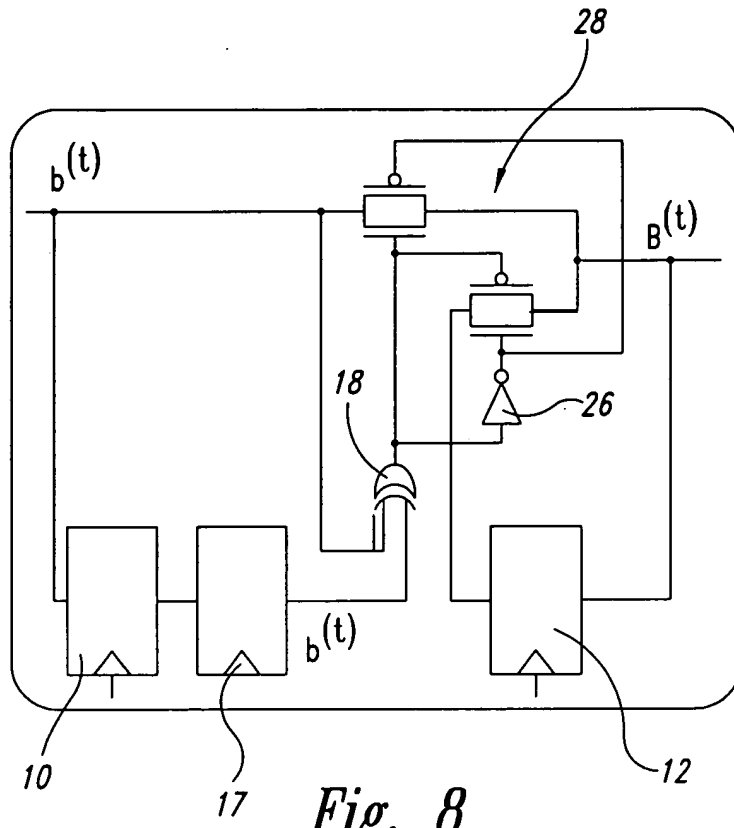
*Fig. 5*



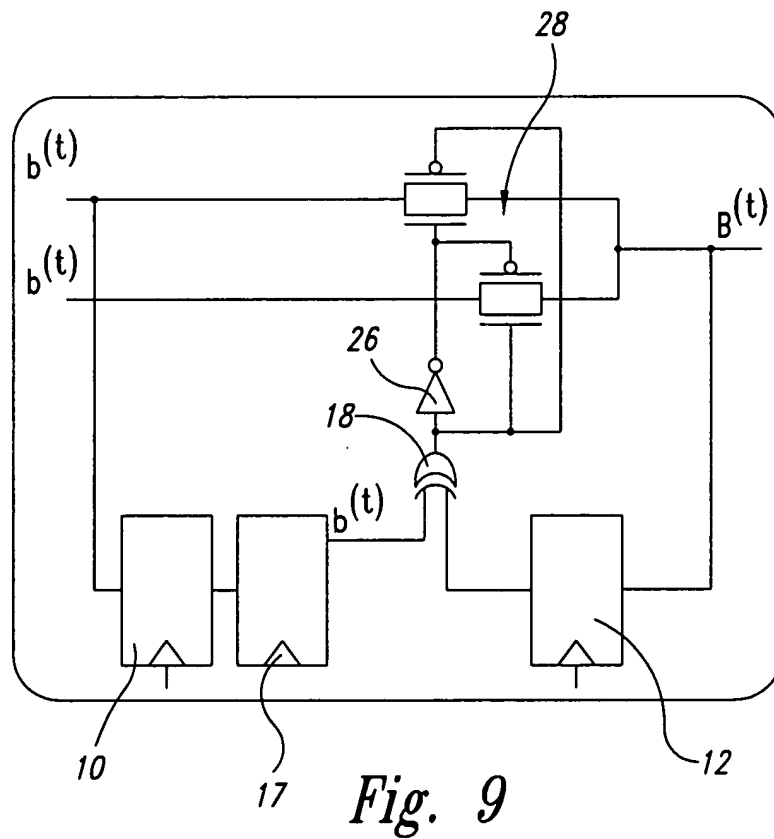
*Fig. 6*



*Fig. 7*



*Fig. 8*



*Fig. 9*